Patent Claims

1. A method for fabricating a memory device (2), which includes semiconductor structures, with memory cells (1), in which digital information is stored in a storage layer (10), in which method:

- two source/drain regions (5), which are spaced apart from one another by a channel region (4), are formed in a semiconductor substrate (17),
- a gate dielectric (6) is provided on a substrate surface of the semiconductor substrate (17), substantially above the channel region (4),

wherein

- a first gate electrode (7a) is arranged on the gate dielectric (6),
- processing of the semiconductor structures is concluded prior to application of the storage layer (10),
- a conductive connection (8) between the storage layer (10) and the first gate electrode (7a) is provided,
- an insulator layer (18) is provided above the storage layer (10), and
- a second gate electrode (7b) is provided on the insulator layer (18).

2. The method as claimed in claim 1, wherein the storage layer (10) is arranged between a first and a second electrode (9a,b).

3. The method as claimed in claim 2, wherein the first electrode (9a) is formed by a portion of the conductive connection (8).

4. The method as claimed in either of claims 2 and 3, wherein one of the metals aluminum, tungsten or copper

is provided for the first and second electrodes (9a, b).

5. The method as claimed in either of claims 2 and 3, wherein one of the precious metals Pt, Au or Ag is provided for the first and second electrodes (9a, b).

6. The method as claimed in one of claims 2 to 5, wherein

- the first electrode (9a) is formed in a first metal level (11a) and the second electrode (9b) is formed in a second metal level (11b), and
- the conductive connection (8) between the first gate electrode (7a) and the first electrode (9a) is produced by a contact hole (14) filled with conductive material.

7. The method as claimed in one of claims 2 to 5, wherein

- the first and second electrodes (9a, 9b) are each formed in a metal level (11) which is in each case processed later in the process sequence, and
- the conductive connection (8) between the first electrode (9a) and the first gate electrode (7a) is produced by contact holes (14) arranged above one another and filled with conductive material.

8. The method as claimed in one of claims 1 to 7, wherein the storage layer (10) provided is an organic layer.

9. The method as claimed in claim 8, wherein the organic layer is provided having porphyrin molecules.

10. The method as claimed in one of claims 1 to 9, wherein

- to produce source and drain lines, the source/drain regions (5) of memory cells (1) arranged in rows which are respectively adjacent within a row are electrically conductively connected to one another by doped regions (16) provided in the semiconductor substrate, and
- after a predetermined number of source/drain regions (5) which have been electrically conductively connected to one another by doped regions (16) in the semiconductor substrate (17), conductive connections (8) to interconnects (13), which are formed in a metal level (11) and connect the source/drain regions (5) of memory cells (1), are provided.

11. A memory cell (1) having a storage layer (10) which stores a digital information item, having two source/drain regions (5), which are formed in a semiconductor substrate (17) and are spaced apart from one another by a channel region (4), and a gate dielectric (6), which is provided on a substrate surface of the semiconductor substrate (17), substantially above the channel region (4),
wherein

- a first gate electrode (7a) is arranged on the gate dielectric (6),
- the storage layer (10) is arranged on the first gate electrode (7a) or at a distance from the first gate electrode (7a),
- a conductive connection (8) between the storage layer (10) and the first gate electrode (7a) is provided,
- an insulator layer (18) is provided above the storage layer (10), and
- a second gate electrode (7b) is provided on the insulator layer (18).

12. The memory cell as claimed in claim 11, wherein the storage layer (10) is arranged between a first and a second electrode (9a, 9b).

13. The memory cell as claimed in claim 12, wherein the first electrode (9a) is formed by a portion of the conductive connection (8).

14. The memory cell as claimed in either of claims 12 and 13, wherein the first and second electrodes (9a, b) consist of one of the metals aluminum, tungsten or copper.

15. The memory cell as claimed in either of claims 12 and 13, wherein the first and second electrodes (9a, b) consist of one of the precious metals Pt, Au or Ag.

16. The memory cell as claimed in one of claims 12 to 15, wherein

- the first electrode (9a) is formed in a first metal level (11a) and the second electrode (9b) is formed in a second metal level (11b), and
- the conductive connection (8) between the first gate electrode (7a) and the first electrode (9a) is provided by a contact hole (14) filled with conductive material.

17. The memory cell as claimed in one of claims 12 to 15, wherein

- the first and second electrodes (9a, b) are each formed in a metal level (11) which is in each case further away from the first gate electrode (7a) than the first or the second metal level (11a, b), and

- the conductive connection (8) between the first electrode (9a) and the first gate electrode (7a) is provided by contact holes (14) which have been introduced into insulation layers (12), are arranged above one another and have been filled with conductive material.

18. The memory cell as claimed in one of claims 11 to 17, wherein the storage layer (10) is provided in the form of an organic layer.

19. The memory cell as claimed in claim 18, wherein the organic storage layer (10) contains porphyrin molecules.

20. A memory device having memory cells which are arranged in rows, include semiconductor structures and store a digital information item, which memory device includes memory cells (1) as claimed in one of claims 11 to 19.

21. The memory device as claimed in claim 20, wherein
- to provide source and drain lines, source/drain regions (5) of memory cells (1) which are respectively adjacent in a row are electrically conductively connected to one another by doped regions (16) provided in the semiconductor substrate (17), and
- after a predetermined number of source/drain regions (5) which have been electrically conductively connected to one another by doped regions (16) in the semiconductor substrate (17), conductive connections (8) to interconnects (13), which are formed in a metal level (11) and connect the source/drain regions (5) of memory cells (1), are provided.

22. A method for operating the memory device (2) as claimed in either of claims 20 and 21, in which:

- to program the memory device (2), the respective storage layers (10) of selected memory cells (1) are charged by means of high-energy electrons or by means of an electron tunnelling operation through the gate dielectric (6) as a result of voltages being applied to the source/drain regions (5) and the second gate electrode (7b),
- to erase the programming, the charged storage layers (10) are discharged by means of an electron tunnelling operation to the channel region (4) or to the source/drain region (5) as a result of an erase voltage, which differs from the voltage applied during programming, being applied to the second gate electrode (7b), and
- to read the programmed memory device (2), the strength of a drain current is detected as a function of a charge state of the storage layer (10).